This listing of the claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Original) A method of forming a microelectronic structure comprising:

forming a sacrificial layer on a hard mask layer disposed on a substrate;

forming a trench in the substrate;

forming a metal layer in the trench of the substrate and on the sacrificial layer;

removing the metal layer until the sacrificial layer is exposed, and wherein a dishing is induced in a top surface of the metal layer; and

then simultaneously removing the metal layer and the sacrificial layer until the dishing in the metal layer is substantially removed without substantially removing the hard mask layer.

2. (Original) The method of claim 1 wherein removing the metal layer wherein a dishing is induced comprises removing the metal layer wherein a dishing depth about equal to or less than the thickness of the sacrificial layer is induced.

3. (Original) The method of claim 1 wherein forming the metal layer in the trench of the substrate and on the sacrificial layer comprises forming a barrier layer in the trench of the substrate and on the sacrificial layer and then forming a metal layer on the barrier layer.

4. (Currently amended) The method of claim 3 wherein forming a barrier layer comprises forming a barrier layer that is from about ~~150~~ 50 to about ~~350~~ 300 angstroms in thickness.

5. (Original) The method of claim 1 wherein forming a sacrificial layer on a hard mask layer disposed on a substrate comprises forming a sacrificial layer disposed on a hard mask layer that is disposed on a dielectric layer.

6. (Original) The method of claim 1 wherein forming a sacrificial layer on a hard mask layer disposed on a substrate comprises forming a sacrificial layer disposed on a hard mask layer that is disposed on a low k dielectric layer.

7. (Original) The method of claim 1 wherein simultaneously removing the metal layer and the sacrificial layer comprises simultaneously removing the metal layer and the sacrificial layer at a removal rate that is at least about 10 times faster than a removal rate of the hard mask layer.

8. (Original) The method of claim 7 wherein simultaneously removing the metal layer and the sacrificial layer at a first removal rate that is at least about 10 times faster than the removal rate of the hard mask layer comprises simultaneously removing the metal layer and the sacrificial layer at a removal rate that is from about 50 to about 100 times faster than a removal rate of the hard mask layer.

9. (Original) The method of claim 1 wherein removing the metal layer until the sacrificial layer is exposed comprises removing the metal layer until a barrier layer is exposed, and then removing the barrier layer until the sacrificial layer is exposed.

10. (Original) The method of claim 1 wherein simultaneously removing the metal layer and the sacrificial layer until the dishing in the metal layer is substantially removed without substantially removing the hard mask layer comprises simultaneously removing the metal layer, a barrier layer disposed on the sacrificial layer, and the sacrificial layer until the dishing in the metal layer is substantially removed without substantially removing the hard mask layer.

11. (Currently amended) The method of claim 1 wherein forming a sacrificial layer comprises forming a sacrificial layer that is from about 300 angstroms to about 1,000 angstroms in thickness.

12. (Currently amended) The method of claim 1 wherein forming a hard mask layer comprises forming a hard mask layer that is from about 50 angstroms to about 400 angstroms in thickness.

13. (Original) A method of forming microelectronic structure comprising:

providing a substrate, the substrate comprising a trench, a metal layer disposed in the trench wherein the metal layer comprises a dishing on a top surface of

the metal layer, and a sacrificial layer disposed on a hard mask layer that is disposed on a first surface of the substrate, and

simultaneously polishing the metal layer and the sacrificial layer until the dishing is removed without substantially removing the hard mask layer.

14. (Original) The method of claim 13 wherein providing a substrate, the substrate comprising a trench, a metal layer disposed in the trench wherein the metal layer comprises a dishing on a top surface of the metal layer, and a sacrificial layer comprises providing a substrate, the substrate comprising a trench, a metal layer disposed in the trench wherein the metal layer comprises a dishing on a top surface of the metal layer, and a sacrificial layer comprising a material selected from the group consisting of non porous spin on glass, undoped silicate glass, tetraethoxysilane, fluorine doped silicon dioxide, carbon doped oxide, silicon carbide, silicon nitride, silicon oxynitride, and silicon carbon nitride, wherein the sacrificial layer is disposed on a hard mask layer that is disposed on a low k dielectric layer.

15. (Original) The method of claim 13 wherein providing a substrate, the substrate comprising a trench, a metal layer disposed in the trench comprises providing a substrate, the substrate comprising a trench, a barrier layer disposed on the trench, and a metal layer disposed on the barrier layer.

16. (Original) The method of claim 15 wherein providing a substrate, the substrate comprising a trench, a barrier layer disposed on the trench, and a metal

layer disposed on the barrier layer comprises providing a substrate, the substrate comprising a trench, a barrier layer comprising at least one of tantalum, tantalum nitride disposed on the trench, and a copper layer disposed on the barrier layer.

17. (Original) The method of claim 13 wherein providing a substrate, the substrate comprising a trench, a metal layer disposed in the trench wherein the metal layer comprises a dishing on a top surface of the metal layer, and a sacrificial layer disposed on a hard mask layer that is disposed on a first surface of the substrate comprises providing a substrate, the substrate comprising a metal layer disposed in a trench wherein the metal layer comprises a dishing on a top surface of the metal layer, a sacrificial layer disposed on a hard mask layer comprising at least one of silicon carbide, silicon nitride, silicon oxynitride, silicon carbon nitride that is disposed on a low k dielectric layer.

18. (Original) A method of forming a microelectronic structure comprising:

providing a substrate comprising a sacrificial layer disposed on a hard mask, and a metal layer disposed in a trench of the substrate and disposed on the sacrificial layer;

removing the metal layer at a first removal rate until the sacrificial layer is exposed and wherein a dishing is induced in a top surface of the metal layer; and

then simultaneously removing the metal layer and the sacrificial layer at a second removal rate without substantially removing the hard mask.

19. (Original) The method of claim 18 wherein removing the metal layer at a first removal rate comprises removing the metal layer utilizing a chemical mechanical process.

20. (Original) The method of claim 18 wherein simultaneously removing the metal layer and the sacrificial layer comprises simultaneously removing the metal layer and the sacrificial layer utilizing a chemical mechanical process.

21. (Withdrawn) An intermediate product comprising:

a metal layer disposed in a trench of a substrate, wherein the metal layer comprises a dishing in a top surface of the metal layer;

a hard mask layer disposed on a first surface of the substrate;

a sacrificial layer disposed on the hard mask layer; wherein the ratio of the thickness of the sacrificial layer to the depth of the dishing in the top surface of the metal layer is equal to or greater than about 1:1.

22. (Withdrawn) The intermediate product of claim 21 wherein the metal layer comprises copper.

23. (Withdrawn) The intermediate product of claim 21 wherein the thickness of the sacrificial layer is from about 300 angstroms to about 1,000 angstroms and comprises a dielectric material.

24. (Withdrawn) The intermediate product of claim 21 wherein the thickness of the hard mask layer is from about 50 angstroms to about 250 angstroms.